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(54) Title: OVERVOLTAGE-PROTECTED I/O BUFFER
 (54) Titre: TAMPON E/S PROTEGE CONTRE LES SURTENSIONS

(57) Abstract

A tristate I/O buffer (101) suitable for cooperation with modules (31) which operate at a higher supply voltage than the supply voltage of the buffer (101). The output (4) of the buffer (101) is provided with an overvoltage protection circuit (110) which prevents current leakage from the output (4) to the supply voltage line (VDD) of the buffer (101). The overvoltage protection circuit (110) comprises a PMOS blocking transistor (120), a first PMOS control transistor (130) and a second NMOS control transistor (140). The two control transistors (130, 140) are controlled by a control signal which is derived solely from the enable signal (E).

(57) Abrégé

Cette invention se rapporte à un tampon E/S à trois états (101) conçu pour coopérer avec des modules (31) qui sont actifs à une tension d'alimentation supérieure à la tension d'alimentation du tampon (101). La sortie (4) du tampon (101) est pourvue d'un circuit (110) de protection contre les surtensions, qui empêche les fuites de courant de la sortie (4) vers la ligne de tension d'alimentation (VDD) du tampon (101). Le circuit (110) de protection contre les surtensions comprend un transistor de blocage PMOS (120), un premier transistor de commande PMOS (130) et un second transistor de commande NMOS (140). Ces deux transistors de commande (130, 140) sont commandés par un signal de commande qui est dérivé uniquement du signal de validation (E).

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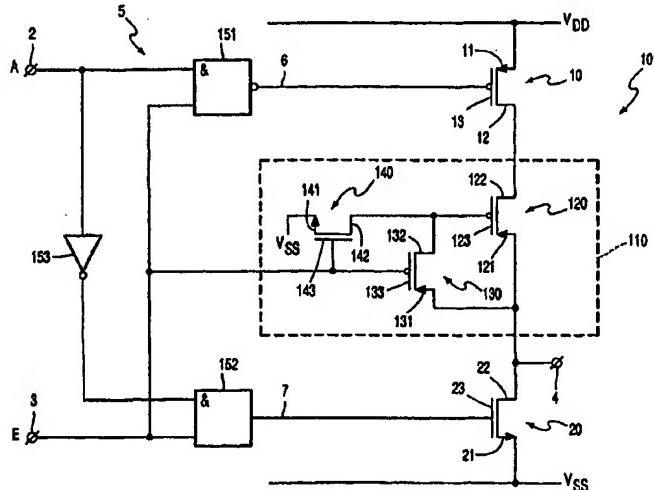
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(21) International Application Number: PCT/EP99/09357 (22) International Filing Date: 1 December 1999 (01.12.99) (30) Priority Data: 98204343.2 18 December 1998 (18.12.98) EP (71) Applicant: KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). (72) Inventors: VAN SCHAIK, Willem, K.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). KALKMAN, Wilhelmus, J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). WIENTJES, Rene, J., M.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). (74) Agent: DUILVESTIJN, Adrianus, J.; Internationaal Octrooibureau B.V., Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).	(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>	

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A tristate I/O buffer (101) suitable for cooperation with modules (31) which operate at a higher supply voltage than the supply voltage of the buffer (101). The output (4) of the buffer (101) is provided with an overvoltage protection circuit (110) which prevents current leakage from the output (4) to the supply voltage line (VDD) of the buffer (101). The overvoltage protection circuit (110) comprises a PMOS blocking transistor (120), a first PMOS control transistor (130) and a second NMOS control transistor (140). The two control transistors (130, 140) are controlled by a control signal which is derived solely from the enable signal (E).

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Description

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Overvoltage-protected I/O buffer.

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The present invention relates to an I/O buffer, and more specifically to a tristate I/O buffer, i.e. a buffer whose output can be in one of the three states: a first state in which the output is actively high, a second state in which the output is actively low and in a third state, also referred to as tristate, in which the output is inactive and this output has a high impedance with respect to the exterior.

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The present invention more specifically relates to an I/O buffer constructed as an IC or forming part of an IC.

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Such logic buffers are generally known and in the active state they produce at their outputs a logic HIGH/LOW level which depends on the logic level received at a data input. An important task of such a buffer is to supply a logic output signal to a load, while a preceding circuit which supplies the data signal is not or hardly loaded. LOW or "0" then corresponds to a first voltage level designated V_{ss} , and generally referred to as "ground" and HIGH or "1" corresponds to a higher second voltage level designated V_{DD} and generally referred to as "supply voltage".

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In many situations of use the output of the tristate buffer is connected to a bus to which at least one input of at least one other logic circuit is connected and to which also one or more outputs of other logic circuits are connected. In such a bus system the logic level of the bus is always determined by one of the connected logic circuits. By means of suitable control circuitry the connected circuits are controlled in such a manner that only one of them can be in an active HIGH/LOW state, the other circuits then being in their tristates in which their outputs consequently present a high impedance with respect to the bus and thus hardly or not affects the HIGH/LOW level supplied by said one circuit.

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Logic circuits are designed for a predetermined supply voltage. A conventional value for this supply voltage is 5 V but recently circuits have been developed for lower supply voltages. Examples of such lower standard supply voltages are 3.0 V and 3.3 V. These circuits have been developed particularly for battery-powered systems such as, for example, a laptop, because the power consumption decreases as the supply voltage is lower. Another reason for the trend towards circuits with a low supply voltage is the fact that there is a continual tendency towards further miniaturization, which means that the dimensions of the circuit

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5 components are constantly reduced. When the supply voltage remains the same the circuit
10 components are exposed to inadmissibly high field strengths.

10 5 However, in practice an apparatus may include several logic circuits designed
for mutually different supply voltages. A reason for this may be, for example, that a version
15 10 for a lower supply voltage has not yet been developed for a given circuit or that the
performance of a version having a higher supply voltage is better. In practice, it therefore
occurs that an I/O buffer is connected to a bus which is also connected to circuits which
20 15 operate at a supply voltage higher than that of this buffer. A situation may arise in which
the buffer is in its tristate condition and the logic level of the bus is HIGH, which is caused by
10 a circuit which operates at such a higher supply voltage, as a result of which the voltage level
appearing at the output terminal of the I/O buffer is higher than its supply voltage level V_{DD}.
In such conditions a current will flow from the output terminal to the supply voltage terminal
of the I/O buffer, which is undesirable. Moreover, the voltage level of the supply voltage V_{DD}
25 15 of the buffer may increase, which is also undesirable. The I/O buffer therefore has a protection
circuit which can prevent such an undesired current.

30 20 An I/O buffer having such an overvoltage protection is described in the
international patent application WO94/29961. Said protection circuit includes two PMOS
transistors, one NMOS transistor and an inverter. The protection circuit is controlled by the
35 25 control signal for the PMOS pull-up transistor and is consequently derived from the data
signal. This has several disadvantages.

40 35 The control signal for the PMOS pull-up transistor is supplied by a logic unit
which in the circuit described in said publication is a NAND gate. In the known circuit this
logic unit serves to control not the PMOS pull-up transistor but also the protection circuit,
45 40 which implies that this logic unit must be capable of supplying comparatively large currents
and should therefore be relatively overproportioned. Moreover, the output of this logic unit is
affected by the switching transients of not only the PMOS pull-up transistor but also those of
the protection circuit, specifically those of the PMOS blocking transistor, which is arranged in
50 45 series with the PMOS pull-up transistor. Since in this known circuit the control signal for the
PMOS pull-up transistor is obtained both on the basis of the enable signal and the data signal,
30 50 while the frequency of the data signal is typically much higher than the frequency of the
enable signal this means that in practice a limitation is imposed on the frequencies at which
said logic unit can operate.

55 The fact that in the known circuit the protection circuit is controlled by a control signal
derived from the data signal means that the protection circuit is switched from the on state to

5 the off state comparatively frequently, which is attended by a comparatively high power dissipation. Moreover, this means that the known circuit responds comparatively slowly to changes of state, which implies a limitation of the frequency range.

10 In the known circuit the gate of the PMOS blocking transistor is controlled via a
15 second PMOS transistor. This second PMOS transistor has its gate connected to the internal supply voltage V_{DD} . When the voltage level at the output of this circuit increases but is only slightly higher than the level of the internal supply voltage V_{DD} said second PMOS transistor will not be driven into full conduction but will tend to keep the PMOS blocking transistor cut off by means of a leakage current. However, this will not wholly succeed, as a result of which
20 a leakage current will also flow from the output to the internal supply V_{DD} via the blocking transistor and the pull-up transistor. Since these transistors are larger than the second PMOS transistor this leakage current will also be larger than the leakage current through the second PMOS transistor. For all the connected tristate buffers this large leakage current must be supplied by the currently active circuit. If the currently active circuit cannot supply such a
25 large leakage current this state will not leave the level to be applied to the bus by the currently active state. The voltage on the bus even remains below the level of the internal supply voltage V_{DD} plus the threshold value for the blocking transistor, as a result of which said leakage current is sustained continuously.

30 It is an object of the invention to eliminate or at least mitigate the above-
35 mentioned drawbacks.

A major object of the present invention is to provide an overvoltage-protected I/O buffer with an improved performance.

A further object of the present invention is to provide an I/O buffer having a smaller number of components.

40 45 50 Another important object of the present invention is to provide an I/O buffer having a protection circuit, in which a control circuit for the protection circuit is derived exclusively from the enable signal.

These and other aspects, features and advantages of the present invention will be elucidated by means of the following description of a preferred embodiment of an I/O buffer in accordance with the present invention with reference to the drawings, in which identical or like elements bear the same reference numerals and in which:

55 Figure 1 diagrammatically illustrates the basic principle of an I/O buffer;

Figure 2 diagrammatically illustrates the structure of a PMOS transistor; and

5 Figure 3 shows the circuit diagram of a preferred embodiment of an I/O buffer
in accordance with the present invention.

10 Figure 1 illustrates the basic principle of an I/O buffer, which as a whole bears
the reference numeral 1. The buffer 1 comprises a PMOS pull-up field-effect transistor 10
15 5 having a source 11, a drain 12 and a gate 13, and an NMOS pull-down field-effect transistor
20 20 having a source 21, a drain 22 and a gate 23. The drain 12 of the PMOS pull-up transistor
25 10 and the drain 22 of the NMOS pull-down transistor 20 are connected to one another and to
30 15 an output terminal 4 for supplying an output signal X. The source 11 of the PMOS pull-up
35 10 transistor 10 is connected to a supply voltage V_{DD} and the source 21 of the NMOS pull-down
40 20 transistor 20 is connected to a reference voltage level V_{SS} , referred to hereinafter as zero level.

20 The PMOS pull-up transistor 10 and the NMOS pull-down transistor 20 are
controlled by a control device 5 having two outputs 6 and 7. The first output 6 of the control
25 device 5 is connected to the gate 13 of the PMOS pull-up transistor 10 and the second output 7
30 15 of the control device 5 is connected to the gate 23 of the NMOS pull-down transistor 20. The
35 control device 5 has a first input 2 for receiving a data signal A, which input will also be
40 20 referred to as the data input. The control device 5 has a second input 3 for receiving an enable
45 25 signal E, which input is also referred to as the enable input. The value of the enable signal
50 30 determines whether the mode of operation of the buffer 1 is "active" or "tristate". Depending
on the implementation the active mode of the buffer 1 may be defined by an enable signal E
whose value is HIGH and the tristate mode of the buffer 1 may be defined by an enable signal
E whose value is low, or the other way around.

35 The control device 5 is adapted to produce a LOW signal at its two outputs 6
and 7 in the active mode of the buffer 1 when the input signal A is HIGH. This causes the
40 25 PMOS pull-up transistor 10 to be driven into conduction, while the NMOS pull-down
45 30 transistor 20 is cut off, as a result of which the voltage at the output terminal 4 is pulled up to
the level V_{DD} .

45 The control device 5 is further adapted to produce a HIGH signal at its two
outputs 6 and 7 in the active mode of the buffer 1 when the input signal A is LOW. This
50 30 causes NMOS pull-down transistor 20 to be driven into conduction, while the primary PMOS
transistor is cut off, as a result of which the output voltage X at the output terminal 4 is pulled
down to the level V_{SS} .

55 In the tristate mode the control device 5 is further adapted to supply a HIGH
signal at its first output 6 and to supply a LOW signal at its second output 7, regardless of the
value of the data signal A, as a result of which the pull-up transistor 10 and the pull-down

5 transistors 20 are both turned off. The PMOS pull-up transistor 10 then forms a high
impedance between the output 4 and the supply voltage V_{DD} , while the NMOS pull-down
transistor 20 forms a high impedance between the output 4 and the zero level V_{SS} . If in this
10 situation the output 4 of the buffer 1 is connected to a bus 30, which is also connected to the
output of a second signal supply means 31 as well as the input of a signal processing means
5 32, the signal supply means 31 can supply its output signal to the signal processing means 32
without any problems, without being hindered by the connected buffer 1, because the output 4
15 forms a high impedance for the bus 30 and consequently does not load the output signal of the
signal supply means 31.

10 If the signal supply means 31 operates at a supply voltage higher than the
supply voltage V_{DD} at which the buffer 1 operates, it may occur that the voltage level of the
bus 30 is higher than the supply voltage V_{DD} . In cases in which owing to external causes the
voltage at the output 4 is higher than the supply voltage V_{DD} , i.e. the voltage at the drain 12 of
the PMOS pull-up transistor 10 is higher than the voltage at the source 11 of this transistor, an
20 undesired leakage current from the drain 12 to the source 11 and, consequently, from the
15 output 4 to V_{DD} , may occur, as will be explained hereinafter.

25 In CMOS technology a PMOS transistor is normally fabricated in an N-type
well. This is illustrated diagrammatically and functionally in Figure 2, in which a substrate as
30 a whole bears the reference numeral 40. In a surface portion of the substrate 40 an N-type well
20 41 is formed. In the N-type well 41 two P+ regions 42 and 43 are formed, which are connected
to a source terminal 52 and a drain terminal 53, respectively. A gate electrode 54 is arranged
35 between the source terminal 52 and the drain terminal 53 and defines a channel region 44
between said two P+ regions 42 and 43 in the surface of the N-type well 41.

40 Furthermore, an N+ region 45 is formed in the N-type well 41 and is connected
25 to an N-well electrode 55, which is connected to the source electrode 52 by an electrical
connection 56.

45 It is to be noted that the structure of such a PMOS transistor is, in principle,
symmetrical, with the proviso that the P+ regions 42 and 43 are substantially identical, as a
result of which, in principle, the source and drain terminals in a circuit may be interchanged.
30 However, the N-well terminal 45 is connected to only one of these two P+ regions 42 and 43
and it is common practice to refer to the P+ region connected to the N+ type N-well terminal
45 as the source.

50 The transition between the P+ region 42 and the N-well region 41 forms a
parasitic POSITION junction 662, which will also be referred to hereinafter as the parasitic

5 source junction 62. In a similar way, the transition between the P+ region 43 and the N-well
10 region 41 forms a parasitic drain junction 63.

If such a PMOS transistor has its source terminal connected to V_{DD} the entire
15 area including the P+ region 42, the N+ region 45 and the N-well region 41 is at the voltage
5 level V_{DD}. If the voltage at the drain terminal 53 is higher than V_{DD} the parasitic drain junction
15 63 is biased in the forward direction. If the difference between the voltage at the drain terminal
53 and the voltage at the source terminal 52 is higher than the threshold voltage of this
parasitic drain junction 63, a current will flow from drain to source and, consequently, from
the bus 30 to V_{DD} in the example of Figure 1.

10 Figure 3 shows an embodiment of an I/O buffer 101 in accordance with the
20 present invention, in which the an overvoltage protection circuit 110 is arranged between the
drain 12 of the PMOS pull-up transistor 10 and the output 4. This overvoltage protection
25 circuit 110 includes a PMOS blocking field-effect transistor 120, a first control field-effect
30 transistor 130 of the PMOS type, and a second control field-effect transistor 140 of the NMOS
35 type. The PMOS blocking transistor 120 has its drain 122 connected to the drain 12 of the
PMOS pull-up transistor 10 and has its source 121 connected to the output 4. The first
40 (PMOS) control transistor 130 has its drain 132 connected to the gate 123 of the PMOS
blocking transistor 120 and has its source 131 connected to the output 4. The second (NMOS)
45 control transistor 140 has its drain 142 connected to the gate 123 of the PMOS blocking
50 transistor 120 and has its source 141 connected to ground V_{SS}. The respective gates 133 and
143 of the two control transistors 130 and 140 receive the enable signal A.

Figure 3 further shows the circuit diagram of an example of the control device
5. In the present example the control device 5 comprises a NAND gate 151, an AND gate 152
and an inverter 153. The NAND gate 151 receives the data signal and the enable signal E at its
25 two respective inputs and its output forms the first output 6 of the control device 5 and is
consequently connected to the gate 13 of the PMOS pull-up transistor 10. The AND gate 152
receives the enable signal E and the data signal A, inverted via the inverter 153, at its two
respective inputs and its output forms the second output 7 of the control device 5 and is
consequently connected to the gate 23 of the NMOS pull-down transistor 20.

When in the active mode (E = HIGH) the data signal A is LOW the level of the
first output 6 of the control device 5 is HIGH, as a result of which the PMOS pull-up transistor
10 is cut off. The level of the second output 7 of the control device 5 is also HIGH, as a result
50 of which the NMOS pull-down transistor 20 conducts. The output 4 is consequently LOW.

5 When in the active mode ($E = \text{HIGH}$) the data signal A is HIGH the level of the
first output 6 of the control device 5 is LOW, as a result of which the PMOS pull-up transistor
10 is conductive. The level of the second output 7 of the control device 5 is also LOW, as a
result of which the NMOS pull-down transistor 20 is cut off. The level of the gate 143 of the
15 second NMOS control transistor 140 is then HIGH, as a result of which the second NMOS
control transistor 140 is conductive and the gate 123 of the PMOS blocking transistor 120 is
pulled to a LOW level, as a result of which this PMOS blocking transistor 120 is also
20 conductive. The level of the gate 133 of the first PMOS control transistor 130 is HIGH, as a
result of which this transistor is cut off. The level at the output 4 is then HIGH.

25 10 In the tristate mode ($E = \text{LOW}$) the level of the first output 6 of the control
device 5 is HIGH, as a result of which the PMOS pull-up transistor 10 is cut off, and the level
of the second output 7 of the control device 5 is LOW, as a result of which the NMOS pull-
down transistor 20 is cut off. The level of the gate 143 of the second NMOS control transistor
140 is then LOW, as a result of which the second NMOS control transistor 140 is cut off. The
25 15 level of the gate 133 of the first PMOS control transistor 130 is low, as a result of which the
first PMOS control transistor 130 is turned on if external sources cause the voltage at the
output 4 to increase, as a result of which the level of the gate 123 of the blocking transistor
120 is pulled up to the level of the source 121 of this, so that this blocking transistor 120 is cut
30 20 off and the comparatively high voltage level of the output 4 cannot reach the PMOS pull-up
transistor 10.

35 35 A major advantage of the circuit proposed by the present invention is that the
gates 151 and 152 of the control device 5 only have to control the pull-up and pull-down
transistors 10 and 20 and are not loaded by components of the overvoltage protection circuit
110.

40 40 25 Another major advantage of the circuit proposed by the present invention is that the switching
state of the components of the overvoltage protection circuit 110 depends exclusively on the
state of the enable signal E and not on the data signal A because the control voltage for the
gates 133, 143 of the two control transistors 130, 140 are derived exclusively from the enable
signal E. Thus, the overvoltage protection circuit 110 of the buffer 101 does not have any
45 30 45 components whose switching state is to be changed in the active mode when the HIGH/LOW
output state changes owing to a HIGH/LOW transition of the data signal A, as a result of
which the buffer 101 can respond comparatively rapidly to changes of the data signal A and
50 50 can therefore handle comparatively high frequencies.

5 An further major advantage of the circuit proposed by the present invention is
that in the tristate mode the gate 133 of the first PMOS control transistor 130 is constantly held
at a LOW level by the enable signal E, as a result of which this first PMOS control transistor
130 is already turned on in the case of small increases of the voltage at the output 4, so that
10 5 even for small increases of the voltage at the output 4 the gate 123 of the blocking transistor
120 is pulled up to the voltage level of the output 4 and, consequently, the blocking transistor
120 is already cut off for small voltage increases at the output 4. This is in contradistinction to
15 the circuit known from WO94/29961, where the blocking transistor is not cut off until the
voltage level at the output is higher than V_{DD} plus the threshold voltage of the first control
10 transistor.

20 Yet another major advantage of the circuit proposed by the present invention is
that the overvoltage protection circuit 110 has only a very small number of components and
that these components can be realized particularly simply during the fabrication of the buffer
101 without the necessity of additional fabrication steps.

25 15 It will be evident to those skilled in the art that the scope of the present
invention is not limited to the examples described hereinbefore but that various alterations and
modifications thereof are possible without departing from the scope of the invention as defined
in the appended Claims.

30 20 For example, it will be evident to those skilled in that art that the logic function
of the control device 5 can be implemented in another manner.

35 Furthermore, it will be evident to those skilled in the art that in the case of
circuits where the tristate mode is characterized by E = HIGH and the active mode is
characterized by E = LOW, the control device 5 can be modified simply by means of inverters
and/or the use of OR/NAND gates in order to achieve the action described hereinbefore.

40 25 Moreover, it will be evident that the invention also relates to an inverting buffer
whose output is HIGH when the data signal A is LOW, and the other way around, in the active
mode.

45 30 Furthermore, it will be evident to those skilled in the art that the invention can
be used not only in a 3 V/5 V environment or 3.3 V/5 V environment but also in other voltage-
level environments. Moreover, the invention is also useful if upon turn-off of a system the
voltage of a supply line can decrease more rapidly than that of an output.

50 Furthermore, it will be evident to those skilled in the art that if the data signal A
and/or the enable signal E are too weak these signals can be amplified by means of buffers.

Claims

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CLAIMS:

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1. A tristate buffer (101) comprising:
 - a control device (5) having a data input (2) for receiving a logic data signal (A), an enable input (3) for receiving a logic enable signal (E), a first control output (6) and a second control output (7);
 - a supply-level line (V_{DD}) and a ground-level line (V_{SS});
 - an output terminal (4);
 - a first field-effect transistor (10) arranged between the output terminal (4) and the supply-level line (V_{DD}) and having a control terminal (13) coupled to the first control output (6) of the control device (5);
 - a second field-effect transistor (20) arranged between the output terminal (4) and the ground-level line (V_{SS}) and having a control terminal (23) coupled to the second control output (7) of the control device (5);
 - an overvoltage protection circuit (110) arranged between the first field-effect transistor (10) and the output terminal (4) and comprising:
 - a third field-effect transistor (120) arranged in series with the first field-effect transistor (10);
 - a fourth field-effect transistor (130) having a control terminal (133) and coupled between a control terminal (123) of the third field-effect transistor (120) and the output terminal (4);
 - a fifth field-effect transistor (140) having a control terminal (143) and coupled to the control terminal (123) of the third field-effect transistor (120);
 - the control device (5) being adapted to cause either the first field-effect transistor (10) to be turned on and the second field-effect transistor (20) to be turned off or the second field-effect transistor (20) to be turned on and the first field-effect transistor (10) to be turned off, in dependence on the value of the logic data signal (A), if the logic enable signal (E) has a first value (HIGH), and to cause both the first field-effect transistor (10) and the second field-effect transistor (20) to be turned off if the value of the logic enable signal (E) has a second value (LOW), characterized in that the overvoltage protection circuit (110) is adapted to cause the fourth field-effect transistor (130) to be turned on, in the situation that both the

5 first field-effect transistor (10) and the second field-effect transistor (20) are turned off, when
the voltage level of the output (4) is higher than the sum of the ground level (V_{SS}) and the
threshold voltage of the fourth field-effect transistor (130); and in that the control terminals
10 (133; 143) of the fourth and the fifth field-effect transistor (130; 140), respectively, are
controlled by a control signal derived exclusively from the enable signal (E).

15 2. A buffer as claimed in Claim 1, wherein the overvoltage protection circuit (110)
is adapted to cause the fourth field-effect transistor (130) to conduct continuously in the
situation in which both the first field-effect transistor (10) and the second field-effect transistor
10 (20) are cut off.

20 3. A buffer as claimed in Claim 1 or 2, wherein the respective control terminals
(133; 143) of the fourth field-effect transistor and the fifth field-effect transistor (130; 140) are
interconnected.

25 4. A buffer as claimed in any one of the Claims 1-3, wherein the respective control
terminals (133; 143) of the fourth field-effect transistor and the fifth field-effect transistor
(130; 140) are controlled by the enable signal (E) itself.

30 20 5. A buffer as claimed in any one of the Claims 1-4, wherein the fifth field-effect
transistor (140) is coupled between the control terminal (123) of the third field-effect transistor
35 (120) and the ground-level line (V_{SS}).

40 6. A buffer as claimed in any one of the preceding Claims, wherein:
25 - the first field-effect transistor (10) is a PMOS pull-up field-effect transistor
having its source (11) connected to the supply-level line (V_{DD}) and having its gate (13)
connected to the first output (6) of the control device (5);
- the second field-effect transistor (20) is an NMOS pull-down field-effect
45 transistor having its source (21) connected to the ground-level line (V_{SS}), having its drain (22)
30 connected to the output (4), and having its gate (23) connected to the second output (7) of the
control device (5);
- the third field-effect transistor (120) is a PMOS blocking transistor having its
50 source (121) connected to the output (4), and having its drain connected to the drain (12) of
the PMOS pull-up field-effect transistor (10);

5 the fourth field-effect transistor (130) is a first PMOS control transistor having its source (131) connected to the output (4), and having its drain (132) connected to the gate (123) of the PMOS blocking transistor (120);

10 the fifth field-effect transistor (140) is a second NMOS control transistor having its source (141) connected to the ground-level line (V_{ss}), and having its drain (142) connected to the gate (123) of the PMOS blocking transistor (120);
5 and wherein the gate (133) of the first PMOS control transistor (130) and the gate (143) of the second NMOS control transistor (140) each receive a control signal derived
15 from the enable signal (E).

10 10
20 7. A buffer as claimed in Claim 6, wherein the gate (133) of the first PMOS control transistor (130) and the gate of the second NMOS control transistor (140) are interconnected and receive the enable signal (E).

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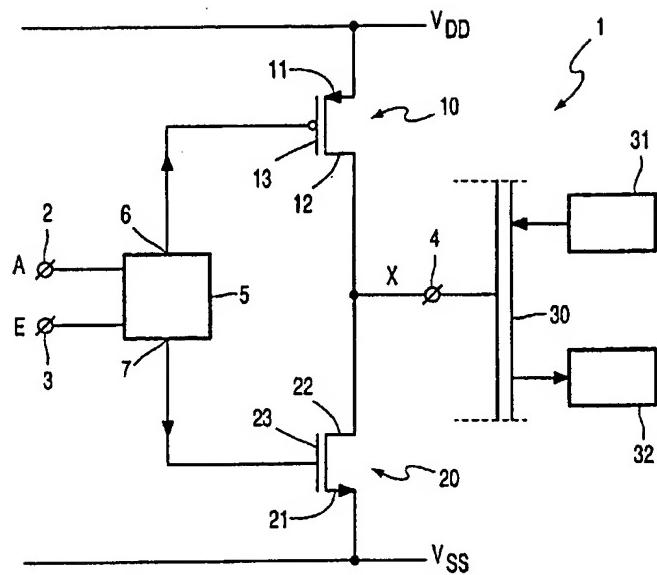


FIG. 1

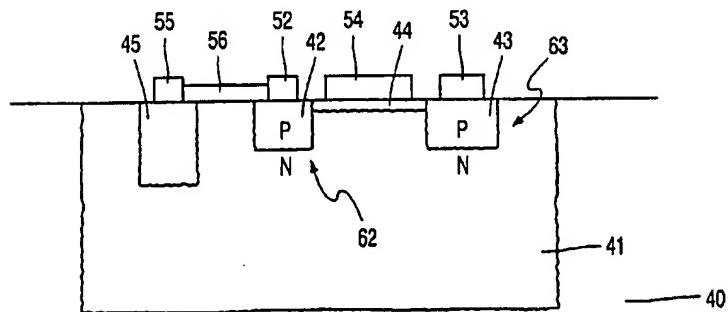
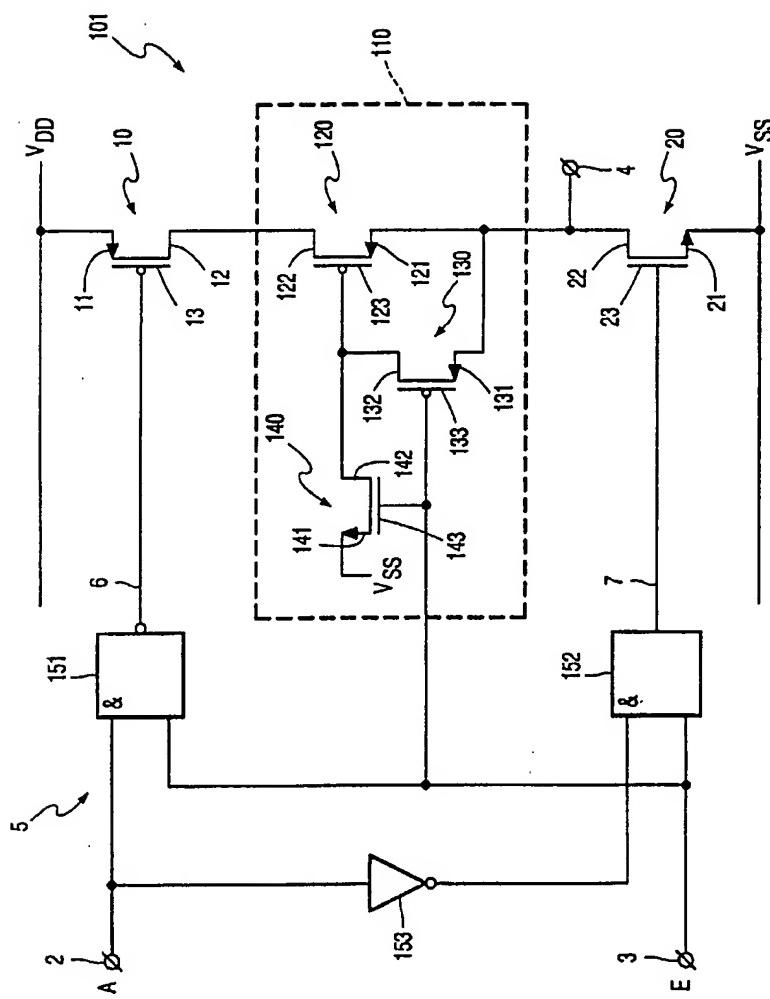


FIG. 2

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FIG. 3



INTERNATIONAL SEARCH REPORT

Int. Serial Application No
PCT/EP 99/09357

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K19/003

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 305 793 A (PMC SIERRA INC) 16 April 1997 (1997-04-16)	1-5
Y	page 4, line 4 -page 7, line 16; figure 1 page 8, line 3 -page 9, line 6; figure 2	6,7
Y	PATENT ABSTRACTS OF JAPAN vol. 1995, no. 11, 26 December 1995 (1995-12-26) & JP 07 202678 A (KAWASAKI STEEL CORP), 4 August 1995 (1995-08-04) abstract	6,7
A	WO 94 18755 A (NAT SEMICONDUCTOR CORP) 18 August 1994 (1994-08-18) figure 4	1-5,7

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the International search

13 March 2000

Date of mailing of the International search report

23/03/2000

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Int'l Application No			
PCT/EP 99/09357			
Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2305793 A	16-04-1997	CA 2171052 A DE 19637013 A FR 2739506 A JP 9116414 A US 5850153 A	30-03-1997 03-04-1997 04-04-1997 02-05-1997 15-12-1998
JP 07202678 A	04-08-1995	NONE	
WO 9418755 A	18-08-1994	US 5343095 A EP 0683937 A US 5387826 A US 5450025 A	30-08-1994 29-11-1995 07-02-1995 12-09-1995